

Abstract

Device for Utilization with the Synchronization of Clock Signals, as well as Clock Signal Synchronizing Method

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The invention relates to a clock signal synchronizing method and to an apparatus device (1) for utilization with the synchronization of clock signals (CLK), comprising delay device (2) with a variably controllable delay time (t_{var}) into which a clock signal (CLK), or a signal obtained therefrom, is input, charged with the variably controllable delay time (t_{var}), and output as a delayed clock signal (DQS),

characterized in that a device (5) is provided for determining whether a clock edge (A') of the delayed clock signal (DQS) output by the delay device (2), or of a signal (FB) obtained therefrom, lies within a predetermined time window before a corresponding clock edge (A) of the clock signal (CLK), or of the signal obtained therefrom.

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